UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/807,567	02/28/1997	RICHARD J. PETROCY	277301	5176

34325 7590 02/17/2011

STANLEY H. KREMEN
4 LENAPE LANE
EAST BRUNSWICK, NJ 08816

EXAMINER	
NORTON, JENNIFER L	
ART UNIT	PAPER NUMBER
2121	

NOTIFICATION DATE	DELIVERY MODE
02/17/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@patentsgroup.com

Office Action Summary	Application No.	Applicant(s)	
	08/807,567	PETROCY ET AL.	
	Examiner	Art Unit	
	Jennifer L. Norton	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application.
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a **Final Office Action** in response to the Amendment/Remarks received on 07 September 2010. Claims 1-6 have been cancelled. Claims 7-18 are newly added. Claims 7-18 are pending in this application.

Petition under the Unintentional Provisions of 37 CFR 1.137(b)

2. A petition under the unintentional provisions of 37 CFR 1.137(b) was filed by Applicant on 07 September 2010, and granted by the Office on 07 October 2010.

Claim Objections

3. Claims 7, 11 and 14 are objected to because of the following informalities:

Claim 7, line 20; claim 11, line 10; and claim 14, line 17 includes the punctuation error "; and,".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 11-13 and 17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject

matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

- As per claim 11, the Applicant has presented the claim limitations "transmits an initial address to the first of the plurality of control units on a first global transmission line of the bus; transmits data on a second global transmission line of the bus; separates data transmission into parts, each part being a packet of data; assigns an address to each packet of data, wherein each said assigned address represents the address of the control unit that will process that packet of data; and retrieves packets of data on a third global transmission line of the signal bus from any one of the plurality of control units by specifying its address on the second transmission line" in claim 11 (See Amendments to the Claims, pg. 2, claim 11), wherein the only support found for this limitation has been found in newly presented claim 11 received by the Office on 07 October 2010.

- As per claim 12, the rejection of claim 11 is incorporated per dependency on claim 11, in addition, the Applicant has presented the claim limitation "a transmitter that sends data packets from every control unit to a key module over the **third transmission line** when the address of that

control unit is specified by the key module" in claim 12 (See Amendments to the Claims, pg. 2, claim 12), wherein the only support found for this limitation has been found in newly presented claim 12 received by the Office on 07 October 2010.

- As per claim 13, the rejection of claim 11 is incorporated as set forth per dependency on claim 11.

- As per claim 17, the Applicant has presented the claim limitation "the control units look to the second global transmission line for an address and read a block of data that is specifically associated with its address" in claim 17 (See Amendments to the Claims, pg. 3, claim 17), wherein the only support found for this limitation has been found in newly presented claim 17 received by the Office on 07 October 2010.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7-18 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,088,008 (hereinafter Reeder) in view of in view of Japan Patent Publication No. 05-173499 (herinafter Atsuo).

7. As per claim 7, Reeder teaches an addressing control unit system for controlling a sequence of or an array of display signs comprising:

a) a plurality of control units (Fig. 12, element 20) each associated with a portion of the display sign array (col. 6, lines 65-67, col. 7, lines 5 and Fig. 1, element 10) and all electrically interconnected by a physical or logical electrical bus (Fig. 12, element 24) having multiple connections (col. 9, lines 22-28 and 34-44 and Fig. 12, element 46);

b) a master or remote controller (Fig. 12, element 18) electrically interconnected with the plurality of control units by the bus (col. 9, lines 18-22 and Fig. 12, element 24);

c) a communication device (i.e. microprocessor) associated with the master or remote controller (col. 4, lines 42-45) for communicating a signal to the plurality of control units along the bus (col. 3, lines 28-31, col. 4, lines 10-13 and col. 9, lines 28-33);

d) a transmission receiver (i.e. logic circuit) within each of the plurality of control units that receives an address (col. 3, lines 17-28 and col. 14, lines 65-67 and col. 15, lines 1-5);

f) memory storage (i.e. memory of the logic circuit) within each of the plurality of control units wherein the address of that control unit is stored internally within the control unit (col. 3, lines 17-28 and col. 14, lines 65-67 and col. 15, lines 1-5); and

control units are interchangeable (col. 4, lines 1-9 and Fig. 12, element 20; display modules), and storing a new address in the memory as its newly present address in the control unit (col. 3, lines 17-28 and col. 14, lines 65-67 and col. 15, lines 1-5).

Reeder does not expressly teach a self-addressing control unit system; a) a physical or logical parallel electrical bus having multiple connections, wherein said bus transfers data or power between the control units;

e) a calculator or computer within each of the plurality of control units wherein the address for that control unit is computed by performing a mathematical operation that changes the address received from the previous control unit;

g) a transmitter within each of the plurality of control units that sends its address to a next control unit; and

whereupon when one of said plurality of control units fails, a new or replacement control unit will be installed and automatically re-address itself in the system by receiving an initial address from a previous or prior control unit, performing the mathematical operation on that initial address to produce a new address, and storing that new address in the memory as its newly present address in the control unit.

Atsuo teaches a self-addressing control unit system (pg. 1-3, par. [0009] [0021] and [0022]);

a) a physical or logical parallel electrical bus having multiple connections, wherein said bus transfers data or power between the control units (Fig. 3);

e) a calculator or computer (i.e. the address-arithmetic circuit 11) within each of the plurality of control units wherein the address for that control unit is computed by performing a mathematical operation that changes the address received from the previous control unit (pg. 2, par. [0010] and [0018]);

d) a transmission receiver (i.e. the address detector 10) within each of the plurality of control units that receives an address from a previous control unit (pg. 2, par. [0010] and [0019]);

g) a transmitter (i.e. transmitting functionality of the address-arithmetic circuit 11) within each of the plurality of control units that sends its address to a next control unit (pg. 2, par. [0010] and [0018]); and

self-configuring and automatic set-up of a control unit (pg. 1-3, par. [0009] [0021] and [0022]) via the control unit addressing itself in the system by receiving an initial address from a previous or prior control unit (pg. 2, par. [0010] and [0019]; i.e. the address detector 10), performing the mathematical operation on that initial address to produce a new address (pg. 2, par. [0010] and [0018]; i.e. the address-arithmetic circuit 11).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Reeder to include a self-addressing control unit system; a) a physical or logical parallel electrical bus having multiple connections, wherein said bus transfers data or power between the control units; e) a calculator or computer within each of the plurality of control units wherein the address for that control unit is computed by performing a mathematical operation that changes the address received from the previous control unit; d) a transmission receiver within each of the plurality of control units that receives an address from a previous control unit; g) a transmitter within each of the plurality of control units that sends its address to a next control unit; and self-configuring and automatic set-up of a control unit via the control unit addressing itself in the system by receiving an initial address from a previous or prior control unit, performing the mathematical operation on that initial address to produce a new address to provide an easy method of setting an address for each display which can simplify a combination activity and maintenance (Atsuo: pg. 1, par. [0007]).

8. As per claim 8, Reeder does not expressly teach the mathematical operation comprises adding a constant to the initial address to produce the new address.

Atsuo teaches the mathematical operation comprises adding a constant to the initial address to produce the new address (pg. 2, par. [0018]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Reeder to include the mathematical operation comprises adding a constant to the initial address to produce the new address to provide an easy method of setting an address for each display which can simplify a combination activity and maintenance (Atsuo: pg. 1, par. [0007]).

9. As per claim 9, Reeder does not expressly teach the constant is one.

Atsuo teaches the constant is one (pg. 2, par. [0018]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Reeder to include the constant is one to produce the new address to provide an easy method of setting an address for each display which can simplify a combination activity and maintenance (Atsuo: pg. 1, par. [0007]).

10. As per claim 10, Reeder teaches as set forth above each control unit includes a non-volatile memory (i.e. an addressable memory) in which it stores its address (col. 3, lines 17-28 and col. 14, lines 65-67 and col. 15, lines 1-5).

11. As per claim 11, Reeder teaches as set forth above the self-addressing control unit system of claim 7 wherein the master or remote controller:

transmits an initial address to the first of the plurality of control units on a first global transmission line of the bus (col. 9, lines 37-43, col. 10, element 61-65 and Fig. 12, element 81);

transmits data on a second global transmission line of the bus (col. 9, lines 37-43 and Fig. 12, element 82);

separates data transmission into parts (Fig. 12, element 82 and 83), each part being a packet of data (col. 9, lines 37-43, col. 10, lines 45-49 and col. 12, lines 39-41);

assigns an address to each packet of data, wherein each said assigned address represents the address of the control unit that will process that packet of data (col. 10, lines 45-49, col. 12, lines 39-41 and Fig. 12, element 83); and,

retrieves packets of data on a third global transmission line of the signal bus from any one of the plurality of control units by specifying its address on the second transmission line (col. 9, line 44, col. 10, lines 52-60 and Fig. 12, element 84).

12. As per claim 12, Reeder teaches as set forth above a transmitter that sends data packets from every control unit to a key module over the third transmission line (col. 9, line 44, col. 10, lines 52-60 and Fig. 12, element 84) when the address of that control unit is specified by the key module (col. 10, lines 45-49 and col. 12, lines 39-41).

13. As per claim 13, Reeder does not expressly teach a control unit has a feedback line to every other control unit.

Atsuo teaches a control unit has a feedback line to every other control unit (Fig. 3).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Reeder to include a control unit has a feedback line to every other control unit to provide an easy method of setting an address for each display which can simplify a combination activity and maintenance (Atsuo: pg. 1, par. [0007]).

14. As per claim 14, Reeder teaches a self-addressing control unit (Fig. 12, element 20)

• that is associated with a portion of a display sign sequence or array (col. 6, lines 65-67, col. 7, lines 5 and Fig. 1, element 10), and

• used in an addressing control unit system (Fig. 12, element 18) for controlling the sequence or array (col. 10, lines 6-17 and 61-65),

• said system having a plurality of control units interconnected by a physical or logical electrical bus (Fig. 12, element 24) having multiple connections (col. 9, lines 22-28 and 34-44 and Fig. 12, element 46),

said control unit comprising:

a) a transmission receiver (i.e. logic circuit) that receives an address (col. 3, lines 17-28 and col. 14, lines 65-67 and col. 15, lines 1-5); and

c) memory storage (i.e. memory of the logic circuit) that stores its new address of the control unit (col. 3, lines 17-28 and col. 14, lines 65-67 and col. 15, lines 1-5).

Reeder does not expressly a self-addressing control unit

• used in a self-addressing control unit system for controlling the sequence or array,

• a physical or logical parallel electrical bus,

• wherein said bus transfers data or power between the plurality of control units, said control unit comprising:

a) a transmission receiver that receives an address from a first other control unit in the system;

b) a calculator or computer that computes a new address for the control unit by performing a mathematical operation that changes the address received from the first other control unit; and

d) a transmitter that sends its new address to a second other control unit.

Atsuo teaches a self-addressing control unit used in a self-addressing control unit system for controlling the sequence or array (pg. 1-3, par. [0009] [0021] and [0022]);

a physical or logical parallel electrical bus having multiple connections (Fig. 3);

wherein said bus transfers data or power between the plurality of control units (Fig. 3);

said control unit comprising:

a transmission receiver (i.e. the address detector 10) that receives an address from a first other control unit in the system (pg. 2, par. [0010] and [0019]);

a calculator or computer (i.e. the address-arithmetic circuit 11) that computes a new address for the control unit by performing a mathematical operation that changes the address received from the first other control unit (pg. 2, par. [0010] and [0018]); and

a transmitter (i.e. transmitting functionality of the address-arithmetic circuit 11) that sends its new address to a second other control unit (pg. 2, par. [0010] and [0018]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Reeder to include a self-addressing control unit used in a self-addressing control unit system for controlling the sequence or array; a physical or logical parallel electrical bus having multiple connections; wherein said bus transfers data or power between the plurality of control units; said control unit comprising: a transmission receiver that receives an address from a first other control unit in the system; a calculator or computer that computes a new address for the control unit by performing a mathematical operation that changes the address received from the first other control unit; and a transmitter that sends its new address to a second other control unit to provide an easy method of setting an

address for each display which can simplify a combination activity and maintenance (Atsuo: pg. 1, par. [0007]).

15. As per claim 15, Reeder does not expressly teach the mathematical operation comprises adding a constant to the address received from the first other control unit to produce its new address.

Atsuo teaches the mathematical operation comprises adding a constant to the address received from the first other control unit to produce its new address (pg. 2, par. [0019] and [0018]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Reeder to include the mathematical operation comprises adding a constant to the address received from the first other control unit to produce its new address to provide an easy method of setting an address for each display which can simplify a combination activity and maintenance (Atsuo: pg. 1, par. [0007]).

16. As per claim 16, Reeder does not expressly teach the constant is one.

Atsuo teaches the constant is one (pg. 2, par. [0018]).

Therefore, it would have been obvious to a person of ordinary skill in the art at

the time of applicant's invention to modify the teaching of Reeder to include the constant is one to produce the new address to provide an easy method of setting an address for each display which can simplify a combination activity and maintenance (Atsuo: pg. 1, par. [0007]).

17. As per claim 17, Reeder teaches as set forth above the control units look to the second global transmission line (Fig. 12, element 82) for an address and read a block of data that is specifically associated with its address (col. 9, lines 37-43).

18. As per claim 18, Reeder teaches a method of networking a plurality of addressing control units for controlling a sequence of or an array of display signs comprising:

a) providing a plurality of control units (Fig. 12, element 20) each containing storage memory (col. 3, lines 17-28 and col. 14, lines 65-67 and col. 15, lines 1-5; i.e. memory of the logic circuit) and each associating with a portion of the display sign array (col. 6, lines 65-67, col. 7, lines 5 and Fig. 1, element 10) and all electrically interconnecting by a physical or logical electrical bus (Fig. 12, element 24) having multiple connections (col. 9, lines 22-28 and 34-44 and Fig. 12, element 46);

b) providing a master or remote control (Fig. 12, element 18) electrically interconnecting with the plurality of control units by the bus (col. 9, lines 18-22 and Fig. 12, element 24);

c) communicating with the master or remote controller for communicating a signal to the plurality of control units along the bus (Fig. 12, element 81) by sending a system start-up signal from the controller to the plurality of control units (col. 9, lines 37-43, col. 10, lines 6-17 and 61-65);

e) control units are interchangeable (col. 4, lines 1-9 and Fig. 12, element 20; display modules), and storing a new address in the memory as its newly present address in the control unit (col. 3, lines 17-28 and col. 14, lines 65-67 and col. 15, lines 1-5).

Reeder does not expressly teach a plurality of self-addressing control units,

a) electrically interconnecting by a physical or logical parallel electrical bus;

d) causing each control unit to calculate an address associated with that control unit by receiving an initial address from a first other control unit, performing a mathematical operation on that address to create a new address, storing the new address in its memory, and transmitting the new address to a second other control unit; and

e) re-addressing whereupon one of said plurality of control units fails, a new or replacement unit will be installed and automatically re-address itself in the system by receiving an initial address from a previous or prior control unit, performing the mathematical operation on that initial address to produce a new address, and storing that new address in the memory as its newly present address in the control unit system.

Atsuo teaches a self-addressing control unit system (pg. 1-3, par. [0009] [0021] and [0022]);

electrically interconnecting by a physical or logical parallel electrical bus (Fig. 3);

causing each control unit to calculate an address associated with that control unit (pg. 2, par. [0010] and [0018]; i.e. the address-arithmetic circuit 11) by receiving an initial address from a first other control unit (pg. 2, par. [0010] and [0019]), performing a mathematical operation on that address to create a new address (pg. 2, par. [0010] and [0018]), and transmitting the new address to a second other control unit (pg. 2, par. [0010] and [0018]); and

self-configuring and automatic set-up of a control unit (pg. 1-3, par. [0009] [0021] and [0022]) via the control unit addressing itself in the system by receiving an initial address from a previous or prior control unit (pg. 2, par. [0010] and [0019]), performing the mathematical operation on that initial address to produce a new address (pg. 2, par. [0010] and [0018]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Reeder to include a self-addressing control unit system; electrically interconnecting by a physical or logical parallel electrical bus; causing each control unit to calculate an address associated with that control unit by receiving an initial address from a first other control unit, performing a mathematical operation on that address to create a new address, and transmitting the new address to a second other control unit; and self-configuring and

automatic set-up of a control unit via the control unit addressing itself in the system by receiving an initial address from a previous or prior control unit, performing the mathematical operation on that initial address to produce a new address to produce a new address to provide an easy method of setting an address for each display which can simplify a combination activity and maintenance (Atsuo: pg. 1, par. [0007]).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references are cited to further show the state of the art with respect to display/signage systems.

U.S. Patent Publication No. 2005/0128100 A1 discloses a protocol for self-addressing control units is effected by arranging a plurality of control units in a sequence and running a data line from a master controller with links to each control unit.

U.S. Patent No. 3,573,790 discloses a solid state circuit controlled variable width character running sign lamp bank including a shift register circuit for each row of lamps in which shift register circuit a pattern of lamp-energizing markers are shifted in accordance with the running sign involved.

U.S. Patent No. 5,254,908 discloses a sign board lighting control system for remotely controlling the lighting of a plurality of sign boards includes a radio transmitting device at a central location, and a radio receiving device and a lighting control unit at each sign board location.

U.S. Patent No. 5,459,477 discloses a display control device according to this invention, video signals are given in parallel each of a plurality of extracting means via a common bus means.

U.S. Patent No. 5,523,769 discloses high resolution large panel displays and more particularly to the utilization of an array of active display modules in which each module is provided with a processing unit to permit rapid painting and updating of the display regardless of display size or pixel density.

U.S. Patent No. 5,530,322 discloses a lighting control system operates to control multiple zones of lighting through multiple dimming circuits so as to achieve any one of several desired lighting scenes.

U.S. Patent No. 5,726,668 discloses a graphics display system including one or more display panels having a plurality of lights, a graphics panel data processor

U.S. Patent No. 5,767,818 discloses a display device which includes a simplified wiring for respective display elements is provided to facilitate the assembly and maintenance.

U.S. Patent No. 5,796,376 discloses an electronic display sign constructed around a system bus architecture.

U.S. Patent No. 6,025,840 discloses a processing system that includes a system master, a system bus coupled to the master, and a plurality of bus interface circuits coupled to bus.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer L. Norton whose telephone number is

(571)272-3694. The examiner can normally be reached on Monday-Friday between 9:00 a.m. - 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Albert DeCady/
Supervisory Patent Examiner
Art Unit 2121

/JLN/